REMARKS

Attorney for Applicant has carefully reviewed the outstanding Office Action on the above-identified application. Applicant has amended the application, as set forth herein, and submits that the application, as amended, is in condition for allowance.

Attorney for Applicant would like to thank Examiners Michelle Estrada and George Fourson for the courtesies extended during a telephone interview conducted on June 3, 2004.

Applicant respectfully traverses the rejection raised in the Office Action under 35 U.S.C. § 112, second paragraph, with respect to the terms "flexible" and "transparent." Applicant submits that these terms are sufficiently clear from their ordinary English language definition, as well as in the specification, to warrant inclusion in the pending claims. "Flexible," as used in everyday English, means capable of being bended. Moreover, this term is sufficiently defined in the specification to comply with the requirements of Section 112, second paragraph. FIG. 2 of the drawings clearly shows the substrates 2 and 10 being flexed during fabrication to provide a finished thin film display. Further, the specification states that the substrates could be spooled off of rolls to allow for high-speed production using flexible substrates (see page 4, lines 28-31). In view of the ordinary English definition of the term "flexible" and the aforementioned disclosure in the specification, Applicant submits that the term "flexible" is sufficiently defined and complies with the requirements of Section 112, second paragraph.

Similarly, Applicant submits that the term "transparent" is likewise sufficiently defined to warrrant inclusion in the pending claims. The ordinary English meaning of the word

"transparent" is capable of transmitting light. The specification clearly points out that the substrates of the present invention could be transparent for transmitting light, so that the present invention could be used in thin-film displays (see, *e.g.*, page 5, lines 29-30 (the top contact of the OLED layer is "transparent to transmit the light, which is emitted from the organic semiconductor.")). Accordingly, Applicant submits that the term "transparent" is sufficiently defined and complies with the requirements of Section 112, second paragraph. Therefore, Applicant respectfully requests withdrawal of the rejection raised in the Office Action with regard to claims 1-17 and 22-25.

Applicant's claimed invention relates to methods for making multi-layer thin-filmed electronics. The invention provides a process for manufacturing macroelectronics comprising the steps of producing thin film active electronics on separate carrier substrates; positioning the thin film active electronics in facing relation; and combining said substrates using anisotropic electrical conductors or light guides so that the thin film active electronics are encapsulated by the anisotropic electrical conductors or light guides. (Claim 1).

The present invention also provides a process for making electronic circuits comprising the steps of forming at least two active circuits on separate carrier substrates; positioning the at least two active circuits in facing relation; and connecting said active circuits with a material which conducts in a direction perpendicular to the separate carrier substrates, wherein the at least two active circuits are encapsulated by the material. (Claim 17).

Further, the present invention provides a method of manufacturing an electronic display comprising the steps of depositing a transparent conductor on a transparent substrate; forming a thin film organic light emitting diode circuit on said transparent conductor; forming a thin film transistor circuit on a second transparent substrate; positioning the organic light emitting diode and thin film transistor circuits in facing relation; and laminating said circuits to each other. (Claim 18).

Further, the present invention provides a method of manufacturing an electronic circuit comprising the steps of forming a first active circuit on a first plane; forming a second active circuit on a second plane; positioning the first and second active circuits in facing relation; and co-laminating said first and second planes with an anisotropic conductor, wherein the anisotropic conductor encapsulates the first and second circuits. (Claim 22).

Additionally, the present invention provides a process for manufacturing macro-electronics comprising the steps of producing thin film active electronics on separate carrier substrates; positioning the active electronics of the carrier substrates in facing relation with respect to each other; and combining said substrates using anisotropic electrical conductors or light guides, the anisotropic electrical conductors or light guides encapsulating the active electronics. (Claim 26).

Finally, the present invention provides a thin film electronic device comprising a first substrate having active electronics formed thereon; a second substrate having active electronics formed thereon, the active electronics of the first substrate positioned in facing relation with the

active electronics of the second substrate; and an anisotropic electrical conductor or light guide positioned between the first and second substrates and encapsulating the active electronics. (Claim 52).

Applicants submit that claims 1, 10, 17, 22, 26, and 35, which were rejected in the Office Action as being anticipated by Japanese Patent No. JP410335830A to Hiramatsu, are patentable over this reference.

Hiramatsu discloses a multilayered printed wiring board and method of manufacture thereof. Each of the circuit boards (see boards 30A, 30B, 30C, and 30D in Drawing 1) are interconnected by a plurality of conductors (see conductors 32a, 32b, 32c, and 32d in Drawing 1). A core substrate is provided between groups of boards (see substrate 20 of Drawing 1). Active electronics can be formed on the exterior surfaces of an outwardly-facing board (see chips 12 and 16 on board 30D in Drawing 1).

Hiramatsu fails to disclose a process for manufacturing macroelectronics comprising the steps of producing thin film **active** electronics on separate carrier substrates; **positioning the thin film active electronics in facing relation**; and combining said substrates using anisotropic electrical conductors or light guides **so that the thin film active electronics are encapsulated by the anisotropic electrical conductors or light guides**, as set forth in amended claim 1. Although Hiramatsu discloses that anisotropic layers can be positioned between the boards of the device, Hiramatsu fails to disclose positioning active electronics on separate carrier substrates in facing relation and encapsulating the active electronics with an anisotropic conductor or light

guide. Indeed, the only mention of active electronics made by Hiramatsu is with regard to chips 12 and 16 (see Drawing 1), and such chips are positioned on the exterior of outwardly-facing board 30D. Hiramatsu is wholly devoid of any disclosure relating to positioning active electronics in facing relation and encapsulating them with an intermediate layer. Moreover, while Hiramatsu discloses the formation of conductors on the boards of the device, such conductors are passive devices and are not active devices. As such, Applicant respectfully submits that claim 1, as amended, is not anticipated by Hiramatsu. Further, claim 10, which contains all of the limitations of amended claim 1, is likewise patentable over Hiramatsu.

Similarly, Hiramatsu fails to disclose each element of Applicant's claimed invention, as set forth in amended claim 17. Hiramatsu fails to disclose a process for making electronic circuits comprising the steps of forming at least two active circuits on separate carrier substrates; **positioning the at least two active circuits in facing relation**; and connecting said active circuits with a material which conducts in a direction perpendicular to the separate carrier substrates, **wherein the at least two active circuits are encapsulated by the material**.

Further, Hiramatsu fails to disclose each element of Applicant's claimed invention as set forth in amended claim 18, which provides a method of manufacturing an electronic display comprising the steps of depositing a transparent conductor on a transparent substrate; forming a thin film organic light emitting diode circuit on said transparent conductor; forming a thin film transistor circuit on a second transparent substrate; **positioning the organic light emitting diode and thin film transistor circuits in facing relation; and laminating said circuits to each other.**

Moreover, Hiramatsu fails to disclose Applicant's claimed invention as set forth in amended claim 22, which provides a method of manufacturing an electronic circuit comprising the steps of forming a first active circuit on a first plane; forming a second active circuit on a second plane; **positioning the first and second active circuits in facing relation**; and co-laminating said first and second planes with an anisotropic conductor, **wherein the anisotropic conductor encapsulates the first and second circuits**.

Additionally, Hiramatsu fails to disclose each element of Applicant's claimed invention as set forth in amended claim 26, which provides a process for manufacturing macroelectronics comprising the steps of producing thin film active electronics on separate carrier substrates; **positioning the active electronics of the carrier substrates in facing relation with respect to each other**; and combining said substrates using anisotropic electrical conductors or light guides, **the anisotropic electrical conductors or light guides encapsulating the active electronics**.

In summary, Hiramatsu fails to disclose each element of Applicant's claimed invention, as set forth in amended claims 1, 17, 18, 22, and 26. Claims 2-16, 19-21, 23-25, and 27-41, which depend from amended claims 1, 17, 18, 22, and 26, respectively, are likewise patentable over Hiramatsu.

In view of the above amendments to independent claims 1 and 26, Applicant submits that claims 2-9 and 27-34, which were rejected in the Office Action as being obvious over Hiramatsu in view of U.S. Patent No. 5,409,798 to Kondo, et al., are patentable over these references. Neither reference, taken alone or in any combination, teaches or suggests positioning active

electronics in facing relation on separate substrates, and encapsulating the active electronics with a material disposed between the substrates, as recited in claims 2-9 and 27-34 by way of Applicant's amendments to independent claims 1 and 26.

Hiramatsu, discussed earlier, fails to teach or suggest positioning active electronics on separate carrier substrates in facing relation, and encapsulating the active electronics with an anisotropic electrical conductor or light guide. Rather, Hiramatsu, discloses positioning active electronics (chips 12 and 16) on an external surface of an outwardly-facing board (see board 30D), and is wholly devoid of any teaching, suggestion, or motivation to provide active electronics on separate carrier substrates and positioning same in facing relation. Further, while Hiramatsu discloses positioning an anisotropic layer between boards of the device, Hiramatsu fails to teach or suggest encapsulating active electronics with an anisotropic conductor.

Kondo, et al. fails to remedy the deficiencies of Hiramatsu. Kondo, et al. provides a plate blank process for producing a printing plate from a plate bank, and a printing method and apparatus using the plate. Kondo, et al. is entirely unconcerned with positioning active electronics in facing relationship and encapsulating such electronics with an anisotropic electrical conductor or light guide, and includes no disclosure relating to electronics. Further, the peeling layer disclosed in Kondo, et al. is incapable of supporting electronics. Moreover, Kondo, et al. relates to an entirely different field of endeavor that the present invention, and as such, is non-analogous art. Therefore, Applicant respectfully submits that claims 2-9 and 27-34, which depend from amended independent claims 1 and 26, are patentable over Hiramatsu in view of Kondo, et al.

In view of the above amendments to independent claims 1, 18, 22, and 26, Applicant submits that claims 11-16, 18-21, 23-25, and 36-41, which were rejected as being obvious over Hiramatsu in view of Kondo, et al. and U.S. Patent No. 5,944,537 to Smith, et al., are patentable over these references. Neither Hiramatsu, Kondo, et al., nor Smith, et al., taken alone or in combination, teach or suggest positioning active electronics in facing relation on separate substrates, and encapsulating the active electronics with a material disposed between the substrates, as recited in claims 11-16, 23-25, and 36-41 by way of Applicant's amendments to claims 1, 22, and 26, nor do the references, taken alone or in combination, teach or suggest positioning the active electronics in facing relation and laminating the active electronics together, as recited in claims 18-21 by way of Applicant's amendments to claim 18.

Hiramatsu fails to teach or suggest positioning active electronics on separate carrier substrates in facing relation, and encapsulating the active electronics with an anisotropic electrical conductor or light guide. Rather, Hiramatsu, discloses positioning active electronics (chips 12 and 16) on an external surface of an outwardly-facing board (see, board 30D), and is wholly devoid of any teaching, suggestion, or motivation to provide active electronics on separate carrier substrates and positioning same in facing relation, and encapsulating active electronics with an anisotropic conductor. Moreover, Hiramatsu fails to teach or suggest laminating such circuits together. Similarly, Kondo, et al. is unconcerned with positioning active electronics in facing relationship, and laminating or encapsulating such electronics with an anisotropic electrical conductor or light guide.

Likewise, Smith, et al., fails to remedy the deficiencies of Hiramatsu and Kondo, et al. Smith, et al. provides a photolithographically patterned spring contact forming an electrical contact between two substrates. Smith, et al. is wholly devoid of any teaching, suggestion, or motivation to position active electronics in facing relation and laminate or encapsulate the active electronics with an anisotropic conductor or light guide. Indeed, Smith, et al. is merely concerned with a mechanical spring contact, and is unconcerned with anisotropic electrical conductors or light guides.

Accordingly, Applicant submits that claims 2-9, 11-16, 18-21, 23-25, 27-34 and 36-41 which depend from amended independent claims 1, 18, 22, and 26, respectively, and contain all of the limitations thereof, are patentable over Hiramatsu, Condo, et al., and Smith, et al., taken alone or in combination.

Applicant has added claims 42-66 to further define the present invention. Claims 42-51 provide that at least one, or both, of the substrates of the present invention is flexible. Further, claims 52-66 recite a thin-film electronic device comprising a first substrate having active electronics formed thereon; a second substrate having active electronics formed thereon, the active electronics of the first substrate positioned in facing relation with the active electronics of the second substrate; and an anisotropic electrical conductor or light guide positioned between the first and second substrates and encapsulating the active electronics. Applicant respectfully submits that these claims are patentable over the cited references.

All issues raised in the Office Action are believed to be addressed. Claims 1, 17, 18, 22, and 26 were amended, and new claims 42-66 have been added. Claims 1-66 are pending in this application, and are believed to be in condition for allowance. No new matter is believed to have been added. Re-examination is requested and favorable action solicited.

Respectfully submitted,

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